



Product Type: Controllers ASC/3 Logic Processor Programming

INTRODUCTION

The Logic Processor provides a means to command the controller inputs and outputs based upon a set of logical statements. This increases the flexibility of the controller and allows the knowledgeable user to implement and verify modifications to the operation of the ASC/3.

Each statement can be controlled by manual data entry (MM-1-8-1) or Time base Action Plan (MM-5-4). It is recommended that the statements that are being developed be programmed in MM-1-8-1 as "D" (disabled). Once the complete operation is developed and ready for evaluation, the statements can be programmed as "E" (enabled). When the statements operate correctly, the statements can be left enabled (E) or put under Time Base action plan (MM-5-4) control (".").

Caution: The controller must be on the bench and not operating an intersection when the Logic Processor is being programmed

There are a total of 200 Logic Processor Statements available for programming. Defining each statement is done in the controller's MM-1-8-2 screens. However, Statements 101-200 must be programmed using the ASC/3 Controller Configurator (formally Mapping Utility) or a special version of NTCIP Data Manager run on a PC. 101-200 can not be accessed on an actual ASC/3 controller.

Statements 1-100 are enabled and disabled via the Controller menus MM-1-8-1 and MM-5-4 as indicated above. Statements 101-200 may only be enabled in a special file called ASC3.EXT.

A detailed explanation of the Extended Logic Processor Groups (statements 101-200) can be found at the end of this document.

The order of Logic Processor statements is extremely critical for proper operation

The ASC/3 executes each statement in once ever 1 / 10 second in a top down starting from logic statement 1. When a logic statement requires information that is developed by another statement, that information must be developed in an earlier statement.

Methods for selecting Logic Processor Testable Elements and Executable Statements are:

- With the cursor the Testable Element (IF Statements) or Executable Statement (THEN or ELSE Statements) column.
 - o Depress the TOGGLE key to select the next element or statement.
 - Depress the "8" key to select the previous element or statement.

If Statements (Testable elements)

The LP (Logic Processor) IF statements can determine the state of selected internal timers, states, CIB (Controller Input Buffer) and COB (Controller Output Buffer) locations. The controller mapping may also determine if the result of the Logic Processor statements to output to the field or get an input from the field. An example of this is if the LP statement is testing Preemption 10 input and there is no connector input pin 00being mapped to that location, the LP statement would never see a change to that location in the CIB.

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Testable	Usable	Test Condition	
Element	Range	Condition	
		PHASE STATE	
	•	are for the se	
	= Need a system		XXXX = Not tested
GREEN ON PHASE	0-16 IS	ON/OFF	
The selected phase (1			
This state for phases 1 YELLOW ON PHASE	0-16 IS	ON / OFF	Dectively.
The selected phase (1			
This state for phases 1			
RED ON PHASE	0-16 IS	ON / OFF	
The selected phase (1			or OFF.
This state for phases 1			
This state is the same			
PHASE TIMING	0-16 IS	ON / OFF	
The selected phase (1			
This state for phases 1			respectively.
PHASE NEXT ON PHS	0-16 IS	ON/OFF	
The selected phase (1			
This state for phases 1 CHECK ON PHASE	0-16 IS also COB	ON / OFF	respectively.
The selected phase (1			chack) is ON or OFF
This state for phases 1			
PED CHECK ON PHAS		ON / OFF	
			destrian demand is ON or OFF.
This state for phases 1			
WALK ON PHASE	0-16 IS	ON / OFF	
The selected active ph			
This state for phases 1			spectively.
PED CLEAR ON PHAS		ON / OFF	
•			destrian clearance is ON or OFF.
This state for phases 1 DON'T WALK ON PHS	0-16 IS also COB	ON / OFF	spectively.
The selected phase (1			
This state for phases 1			
OMIT ON PHASE	0-16 IS	ON / OFF	
The selected phase (1			N or OFF.
This state for phases 1			
PED OMIT ON PHASE	0-16 IS	ON / OFF	
The selected phase (1			
This state for phases 1			espectively.
HOLD ON PHASE	0-16 IS	ON / OFF	
The selected phase (1	-16) or any (0) p	nase hold is ON	N OF UFF.





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This state for phases 1-16 is also CIB code 80-95 respectively.

FORCE OFF ON PHASE 0-16 IS ON / OFF

The selected phase (1-16) or any (0) phase has ON forced off is or OFF.

This state indicated when the selected phase (1-16) or any (0) green has been forced off. This testable element is true during the yellow Change and Red Clearance of the selected phase.

CALL ON PHASE 0-16 IS ON / OFF

The selected phase (1-16) or any (0) phase check is ON or OFF if it part of the active sequence. "CALL ON PHASE" does not indicate true if the phase is not part of the active sequence or omitted for any reason, This include an input, Coordinator, Preemptor, Time Base programming along with any other feature that omits the phase

The state for phases 1-16 can be determined by LP statement COB CODE ON/OFF 352-367 respectively for any phase that is in the sequence even if it omitted.

PED CALL ÓN PHÁSE 0-16 IS ON / OFF

The selected active phase (1-16) or any (0) phase pedestrian check is ON or OFF. "PED CALL ON PHASE does not indicate true if the phase pedestrian movement is not part of the active sequence or is omitted for any reason, This include an input, Coordinator, Preemptor, Time Base programming along with any other feature that omits the phase pedestrian movement. This state for pedestrian omits 1-16 is also CIB code 360-383 respectively.

DET FAIL ON PHASE 0-16 IS ON / OFF

The selected active phase (1-16) or any (0) phase failed detector is ON or OFF.







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RING TIMERS

(These timers are for any phase timing in the selected ring)

To determine when a timer is equal to a partial second, set a flag on the next higher value and delay the partial second required.

* Example. (Determine when Minimum green for phase 1 (ring 1) has 1.2-seconds left. This will function only if stop time or manual advance is not applied during the delay period.

IF MIN GREEN TME RING 1 IS 2

AND GREEN ON PHASE 1 IS ON (True for 1/10 second) THEN SET LOGIC FLAG 1 ON

IF LOGIC FLAG 1 IS ON

THEN DELAY FOR 0.8

(Insert what ever statements that you wish to become active when 1.2 seconds are left in phase 1 minimum green. <u>Be sure to clear the logic flag 1 when it is no longer required</u>.)

MIN GRN TMR RING1

A phase in RING 1 is timing minimum green down from the programmed value to zero in tenths of seconds. The value is entered in seconds. *

MAX GRN TMR RING1 IS, !=, > or < 0-255

A phase in RING 1 is timing max green down from the programmed value to zero in tenths of seconds. The value is entered in seconds. *

IS, !=, > or < 0-255

When in a phase is green with no conflicting demand, the Max Green Timer is set to zero.

YELLOW TMR RING1 IS, !=, > or < 0-255

A phase in RING 1 is timing yellow change expressed in second intervals from 25.5 to 0.0. This value counts down. *

RED TIMER RING1

IS, !=, > or < 0-255

A phase in RING 1 is timing red clearance down from the programmed value to zero in tenths of seconds. The value is entered in seconds. *

WALK TIMER RING1 IS, !=, > or < 0-255

A phase in RING 1 is timing walk down from the programmed value to zero in tenths of seconds. The value is entered in seconds. *

PCLR TIMER RING1 IS, !=, > or < 0-255

A phase in RING 1 is timing pedestrian clearance down from the programmed value to zero in tenths of seconds. The value is entered in seconds. *

MIN GRN TMR RING2 IS, !=, > or < 0-255

A phase in RING 2 is timing minimum green down from the programmed value to zero in tenths of seconds. The value is entered in seconds. *

MAX GRN TMR RING2 IS, !=, > or < 0-255

A phase in RING 2 is timing max green . down from the programmed value to zero in tenths of seconds. The value is entered in seconds. *

YELLOW TMR RING2 IS, !=, > or < 0-255

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ASC/3 Logic Processor Programming A phase in RING 2 is timing yellow change expressed in 1/10 second intervals from 25.5 to 0.0. down from the programmed value to zero in tenths of seconds. The value is entered in seconds. * **RED TIMER RING2** IS, !=, > or < 0-255 A phase in RING 2 is timing red clearance expressed down from the programmed value to zero in tenths of seconds. The value is entered in seconds. * This value counts down. WALK TIMER RING2 IS. !=. > or < 0-255 A phase in RING 2 is timing walk down from the programmed value to zero in tenths of seconds. The value is entered in seconds. * This value counts down. IS. !=. > or < 0.255PCLR TIMER RING2 A phase in RING 2 is timing pedestrian clearance down from the programmed value to zero in tenths of seconds. The value is entered in seconds. * This value counts down. MIN GRN TMR RING3 IS, !=, > or < 0.255A phase in RING 3 is timing minimum green down from the programmed value to zero in tenths of seconds. The value is entered in seconds. * This value counts down. MAX GRN TMR RING3 IS, !=, > or < 0-255 A phase in RING 3 is timing max green down from the programmed value to zero in tenths of seconds. The value is entered in seconds. * This value counts down. YELLOW TMR RING3 IS, !=, > or < 0.255A phase in RING 3 is timing yellow change down from the programmed value to zero in tenths of seconds. The value is entered in seconds. * This value counts down. **RED TIMER RING3** IS. !=. > or < 0-255 A phase in RING 3 is timing red clearance down from the programmed value to zero in tenths of seconds. The value is entered in seconds. * This value counts down. WALK TIMER RING3 IS, !=, > or < 0.255A phase in RING 3 is timing walk down from the programmed value to zero in tenths of seconds. The value is entered in seconds. * This value counts down. IS, !=, > or < 0-255 PCLR TIMER RING3 A phase in RING 3 is timing pedestrian clearance down from the programmed value to zero in tenths of seconds. The value is entered in seconds. * This value counts down. MIN GRN TMR RING4 IS, !=, > or < 0-255 A phase in RING 4 is timing minimum green down from the programmed value to zero in tenths of seconds. The value is entered in seconds. * This value counts down. IS, !=, > or < 0-255 MAX GRN TMR RING4 A phase in RING 4 is timing max green down from the programmed value to zero in tenths of seconds. The value is entered in seconds. * This value counts down. YELLOW TMR RING4 IS, !=, > or < 0.255A phase in RING 4 is timing yellow change down from the programmed value to zero in tenths of seconds. The value is entered in seconds. * This value counts down. **RED TIMER RING4** $|S_{.}| = ... > or < 0.255$ A phase in RING 4 is timing red clearance down from the programmed value to zero in tenths of seconds. The value is entered in seconds. * This value counts down. WALK TIMER RING4 IS, !=, > or < 0-255 A phase in RING 4 is timing walk down from the programmed value to zero in tenths of seconds. The value is entered in seconds. * This value counts down. PCLR TIMER RING4 IS, !=, > or < 0.255

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A phase in RING 4 is timing pedestrian clearance down from the programmed value to zero in tenths of seconds. The value is entered in seconds. * This value counts down.

RING INPUTS (These inputs are for the selected ring)

INHIBIT MAX RING 0-4 IS ON / OFF Inhibit max input to the selected ring (1-4) or any ring (0) is ON or OFF. This state for MAX INHIBIT inputs for rings 1,2,3,4 are also CIB code 128, 136, 144, 152 respectively. MAX 2 RING ON / OFF 0-4 IS Max 2 is input to the selected ring (1-4) or any ring (0) is ON or OFF. This state for MAX 2 inputs for rings 1,2,3,4 are also CIB code 129, 137, 145, 153 respectively. MAX 3 RING 0-4 ON / OFF IS Max 3 is input to the selected ring (1-4) or any ring (0) is ON or OFF. This state for MAX 3 inputs for rings 1,2,3,4 are also CIB code 130, 138, 146, 154 respectively. **OMIT RED CLR RING** 0-4 IS ON / OFF Omit red clearance input to the selected ring (1-4) or any ring (0) is ON or OFF. This state for OMIT RED CLEARANCE inputs for rings 1,2,3,4 are also CIB code 131, 139, 147, 155 respectively. RED REST RING 0-4 IS ON / OFF Red rest input to the selected ring (1-4) or any ring (0) is ON or OFF. This state for RED REST inputs for rings 1,2,3,4 are also CIB code 132, 140, 148, 156 respectively. 0-4 ON / OFF PED RECYCLE RING IS Pedestrian recycle input to the selected ring (1-4) or any ring (0) is ON or OFF. This state for PED RECYCLE inputs for rings 1,2,3,4 are also CIB code 133, 141, 149, 157 respectively. FORCE OFF RING 0-4 IS ON / OFF Force off input to the selected ring (1-4) or any ring (0) is ON or OFF. This state for FORCE OFF inputs for rings 1,2,3,4 are also CIB code 134, 142, 150, 158 respectively. STOP TIME RING 0-4 IS ON / OFF Stop Time input to the selected ring (1-4) or any ring (0) is ON or OFF. This state for STOP TIME inputs for rings 1.2,3,4 are also CIB code 135, 141, 149, 157 respectively. **OVERVERLAP STATE** (These states are for the selected overlap) ON / OFF **OVERLAP** 0-16 IS Overlap A-P (1-16 respectively) or any overlap (0) is active. OVERLAP GREEN ON / OFF 0-16 IS Overlap A-P (1-16 respectively) or any overlap (0) is green. This state for overlap A-P (1-16 respectively) green is also COB code 96-111 respectively. If the overlap green to be tested is turned ON or OFF by a previous LP statement, the use of

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"COB CODE ON" or "COB CODE OFF" (96-111 respectively) should be used in subsequent LP statements.

OVERLAP GREEN EXT0-16ISON / OFFOverlap A-P (1-16) or any overlap (0) is timing lag or trailing green.OVERLAP YELLOW0-16ISON / OFF

Overlap A-P (1-16) or any overlap (0) is yellow.

This state for overlap A-P (1-16 respectively) Yellow is also COB code 112-127 respectively.

OVERLAP RED CLR 0-16 IS ON / OFF						
Overlap A-P (1-16) or any overlap (0) is in red clearance.						
OVERLAP RED 0-16 IS ON / OFF						
Overlap A-P (1-16) or any overlap (0) is red.						
This state for overlap A-P (1-16 respectively) Red is also COB code 96-111 respectively.						
NOTE: OVERLAP RED 0 will be true unless all overlaps are either green or yellow. Any non-						
programmed overlap will be red						
OVERLAP OMIT 0-16 IS ON / OFF						
Overlap A-P (1-16) or any overlap (0) omit is ON or OFF.						
This state for overlap A-P (1-16 respectively) Red is also CIB code 464-479 respectively.						
OVERLAP WALK 0-16 IS ÓN / OFF						
Overlap walk 1-16 or any overlap (0) Walk is ON or OFF.						
An Overlap Walk is a ped overlap enabled in MM-2- 3 even if it is only one phase.						
OVERLAP PED CLEAR 0-16 IS ON / OFF						
Overlap walk 1-16 or any overlap (0) Ped Clearance is ON or OFF.						
An Overlap Ped Clearance is a ped overlap enabled in MM-2- 3 even if it is only one phase.						
OVERLAP DON'T WALK 0-16 IS ON / OFF						
Overlap walk 1-16 or any overlap (0) Don't Walk is ON or OFF.						
An Overlap Don't Walk is a ped overlap enabled in MM-2-3 even if it is only one phase.						
The Ped Overlap must be comprised of at least one phase the at has a enabled pedestrian						
movement. If it does not, the Don't Walk will not be sensed.						
The Ped Overlap Don't Walk will toggle at 1 PPS during the Pedestrian clearance.						
COORDINATOR STATES						
(States of the coordinator)						

COORD FLASH

IS ON / OFF

The coordinator is commanding flash (Pattern 255)

COORD FREE IS ON/OFF

The coordinator is commanding free (Pattern 254)

The Coordinator Free Status (by any command can be determined by COB CODE 454 ON/OFF If the NIC commanded free is required, set a Special Function output when that Action Plan is in effect and test for that output. COB CODE 512-519 ON/OFF for NIC special functions 1-8 respectively

COORD IN STEP

IS ON/OFF

The coordinator is commanded to a pattern even if is free.

COORD PLAN 1-63 IS, !=, > or < 0-120







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The coordinated plan in effect IS, !=, > or < the programmed value even if the coordinator is free. **CYCLE LENGTH** IS, !=, > or < 0.999The cycle length in effect IS, !=, > or < the programmed value even if the coordinator is free. OFFSET IS, !=, > or < 0.255The offset in effect IS, !=, > or < the programmed value even if the coordinator is free. RESERVED (not used). IS, !=, > or < 0-2047 LOCAL CYCLE TIMER The local cycle timer IS, !=, > or < the programmed value in tenths of seconds. MASTER CYCLE TIMER IS, !=, > or < 0-999 The master cycle timer IS, !=, > or < the programmed value in seconds. IS, !=, > or < 0-2047 SPLIT TIMER RING 1-4 The split timer for ring (1-4) or any ring (0) IS (!=, > or <) the programmed value in seconds. To determine the split timing for a specific phase, use the following: IF PHASE TIMING 4 IS ON AND SPLIT TIMER RING 1 < 10 seconds PREEMPTOR STATES (States and inputs of the preemptor)

PREEMPT INPUT 0-10 IS ON / OFF

The selected preempt (1-10) or any preempt (0) input is active. This is regardless of the programming for that preemptor.

PREEMPT ACTIVE 0-10 IS ON / OFF

The selected preempt (1-10) or any preempt (0) is active.

WAIT FOR PREEMPT IS ON / OFF

There is no preemptor active and the controller will respond to the next preemption input. This feature is true during delay timing, all during preemption. It is not true when the controller is not in preemption or an input is inhibited because of reservice timing.

PREEMPT DELAY IS ON / OFF

There is a preemptor delay timing and there is no active preemptor,

PMT ADV TRACK CLR IS ON / OFF

There is a preemptor timing entrance green, walk, pedestrian clearance, yellow or all red and there is a track clearance movement.

PMT TRACK CLEAR IS ON / OFF

The active preemptor is timing Track Clearance intervals green, yellow and all red.

PMT ADVNCE TO HOLD IS ON / OFF

Indicated that the preemptor is starting to time the Cycling / Dwell phases.

PREEMPT DWELL IS ON / OFF

The active preemptor is timing dwell phases.

PREEMPT CYCLING IS ON / OFF

The active preemptor is timing cycling phases.

PREEMPT CYC DELAY IS ON / OFF

The Preemptor is timing the Extend Input time during Dwell / Cycling phases

PRMPT ADV TO FLASH IS ON / OFF



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The active preemptor is timing Track Clearance intervals yellow, all red and the preemptor will flash the dwell phases yellow and others red. **PREEMPT FLASH** IS ON / OFF The Preemptor is being held during the Extend Input timing. This statement is true when the Extend timer is timing and the preemption is in Dwell Flash.

PRMPT FLASH DELAY IS ON / OFF The Preemptor is timing the Extend Input time during dwell flash

I ne Preemptor is timing the Extend input time during dwell fi

PRMPT ADV TO EXIT IS ON / OFF

The preemption is preparing to exit. The PMT call is false, Minimum Dwell and Duration times are complete

PRMPT RESRV TIMER 0-10 IS, !=, > or < 0-2047

The Preemption reservice time is tested against a particular value

PRMPT DELAY TIMER 0-10 IS, !=, > or < 0-2047

Time is entered in seconds for Preemptor 1-10 or any Preemptor "0" delay

PRMPT MAX CALL TMR IS, !=, > or < 0-255

The maximum time that a non-priority preemption call can be active and be recognized by the controller. Once failed, the input must return to inactive state to be recognized again.

PRMPT DURRATION TMR IS, !=, > or < 0-255

The Duration Timer for the preemptor in effect is compared against the entered value and the statement is set true when the selected conditions are true

PMT MIN DWELL TIMER IS, !=, > or < 0-255 The Dwell Timer for the preemptor in effect is compared against the entered value and the statement is set true when the selected conditions are true

PMT TRACK GRN TMR IS, !=, > or < 0-255

The Track Clearance Green Timer for the preemptor in effect is compared against the entered value and the statement is set true when the selected conditions are true

PMT HOLD GREEN TMR IS, !=, > or < 0-255

The Preemptor is being held during the Extend Input timing. This statement measures the Extend timer.

- PMT CYC DLY TMR
- IS, !=, > or < 0-255







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DETECTOR STATES

(States and inputs of the vehicle and pedestrian detectors)

DETECTOR	1-64	IS	ON / OFF
The selected vehicle of	letector (1-6	4) is Ol	N or OFF when the detector is assigned to a phase.
			or OFF that not assigned to a phase, use the CIB CODE
ON/OFF 0-63 for dete			•
DETECTOR FAIL	1-64	ıs	ÓN / OFF
	letector (1-6	4) failu	re is ON or OFF when the detector is assigned to a phase.
When not assigned to			
DETECTOR DELAY T		IS	ON / OFF
			ning delay when the detector is assigned to a phase.
			ctor delay does not time.
		IS	ON / OFF
	-	-	is timing when the detector is assigned to a phase. When
not assigned to a phase. The			
PED DETECTOR	0-16	IS	ON / OFF
		-	
			detector is on or off ON or OFF when the detector is
			a ped movement programmed.
			or OFF that not assigned to a phase, use the CIB CODE
ON/OFF 64-79 for de			
PED ABSENCE FAIL	0-16	IS	ON / OFF
	any (0) ped	lestrian	detector has failed because of no activity. Reference MM-
6-7.			
PED LOCK FAIL	0-16		ON / OFF
· · · · ·	any (0) ped	lestrian	detector has failed because of max presence.
Reference MM-6-7.			
PED ERRATIC FAIL	1-16	IS	ON / OFF
· · · ·	edestrian det	tector h	nas failed because of excessive counts.
Reference MM-6-7.			
DETECTOR VOLUME	1-64	IS, !=,	, > or < 0-2047
The selected (1-64) ve	hicle detect	or volu	me count for an enabled detector (MM-6-2) that was
collect during the last	NTCIP Log F	Period	(MM-6-5).
0-254 = The volume d	ata collected	d.	
255 = The volume of t	he data colle	ected is	s greater than 254.
DET OCCUPANCY %	1-64	IS, !=,	, > or < 0-999
The selected (1-64) ve	hicle detect	or occu	upancy in 0.5 % increments for an enabled detector (MM-6-
2) that was collect dur			
			Enter the occupancy level that is being tested times 2. (i.e.
0 = 0%, 36 =			
210 = Max Presence I	•	-,	
211 = No Activity Faul			
212 = Open Loop Fau			

- 213 = Shorted Loop Fault
- 214 = Excessive Change Fault







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216 = Watchdog Fault

217 = Erratic count Fault

Note: The highest number is reported when there is more than one fault active.

MISC STATES (Miscellaneous and TOD states)

TOD MONTH

IS, !=, > or < 1-12

Determines if the TOD Month is equal to, not equal to, greater than or less than the compared to value.

TOD DOM

|S, !=, > or < 1-31

Determines if the TOD Day of Month is equal to, not equal to, greater than or less than the compared to value.

TOD DAY OF WEEK

 $|S_{.}| = ... > or < 1-7$

Determines if the TOD Day of Week is equal to, not equal to, greater than or less than the compared to value. Sunday is day 1 for this comparison. IS. !=. > or < 0.23

TOD HOUR

Determines if the TOD Hour is equal to, not equal to, greater than or less than the compared to value. Sunday is day 1 for this comparison. IS, !=, > or < 0-59

TOD MINUITE

Determines if the TOD Day of Week is equal to, not equal to, greater than or less than the compared to value. Sunday is day 1 for this comparison. IS, !=, > or < 0.59

TOD SECOND

Determines if the TOD Day of Week is equal to, not equal to, greater than or less than the compared to value. Sunday is day 1 for this comparison.

TOD TENTH SEC IS, !=, > or < 0.9

Determines if the TOD Day of Week is equal to, not equal to, greater than or less than the compared to value. Sunday is day 1 for this comparison.

- LOGIC FLAG 1-64 IS ON / OFF
 - Determines if a logic flag is ON (set) or OFF (reset).

The logic flags are not automatically reset except at power on. When used, a LP statement when no longer required must reset them.

LOGIC STATEMENT ON / OFF 1-64 IS

Determines if a logic statement is enabled from any source. These sources are Manually (MM-1-8-1) and if allowed, by the action plan in effect (M-5-4).

CIB CODE OFF 0-575

Checks if the state of the selected CIB bit number (0-575) is OFF.

CIB CODE ON 0-575

Checks if the state of the selected CIB bit number (0-575) is ON.

COB CODE OFF 0-767

Checks if the state of the selected COB bit number (0-767) is ON.

COB CODE ON 0-767

Checks if the state of the selected COB bit number (0-767) is OFF.

SPLIT PATTERN 1-120 IS

Checks if split pattern (1-120) is in effect.

DET PLAM NUM IS 1-4



Checks if detector plan (1-4) is in effect. DAY PLAN NUMBER IS 1-16 Checks if day plan (1-64) is in effect. ACTION PLAN NUM IS 1 - 100Checks if action plan (1-100) is in effect. DAY PLAN NUMBER IS 1-4 Checks if controller (1-4) is in effect. SEQUENCE NUMBER IS 1-16 Checks if sequence (1-16) is in effect. TIMEPLAN IN EFFECT IS 1-4 Checks if timing plan (1-4) is in effect. PH RECALL PLAN IS 1-4 Checks if phase recall plan (1-4) is in effect. BIKE CALL ON PHASE ON / OFF 1-16 IS Checks if bike call on phase (1-16) is on or off. (blank) This is a "Do Nothing" Statement.

Then - Else Statements (Executable Statements)

The LP (Logic Processor) Then - Else Statements set or clears the CIB (Controller Input Buffer) and COB (Controller Output Buffer) and internal locations. The controller mapping determines if the results of these statements result in an output to the field or input from the field. An example of this is if the LP statement is sets PHASE GREEN 16 ON and no pin is mapped to that function, there will be no output.







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Executable	Usable	Set
Statement	Range	Condition

DELAY FOR 0.0-204.7 SECONDS

Delay for the entered time before the following statements will be executed.

SET LOGIC FLAG 0-63 ON / OFF

Set LOGIC flag ON or OFF. Once set, the Logic Flag will remain on until turned off.

PHASE OUTPUTS (These outputs are for the selected phase)

SET PHASE GREEN 0-16 ON / OFF

Set the phase green output ON or OFF. The state of the green output will return to the phase state every tenth second. To keep the output ON or OFF, the logic processor must turn it ON or OFF every tenth second.

SET PHASE GREEN 1-16 ON/OFF is the same as SET COB ON/OFF 0-15 respectively and only sets the TS1 and TS2 Type 2 outputs. It is suggested that the Load Switch Green / Walk channel also be set ON or OFF using **SET LDSW GRN/WLK** 0-16 ON / OFF

SET PHASE YELLOW 0-16 ON / OFF

Set the phase yellow output ON or OFF. The state of the green output will return to the phase state every tenth second. To keep the output ON or OFF, the logic processor must turn it ON or OFF every tenth second.

SET PHASE YELLOW 1-16 ON/OFF is the same as SET COB ON/OFF 16-31 respectively. and only sets theTS1 and TS2 Type 2 outputs. It is suggested that the Load Switch Yellow / Ped Clearance channel also be set ON or OFF using **SET LDSW YEL/PDCL 0-16 ON / OFF**

SET PHASE RED 0-16 ON / OFF

Set the phase red output ON or OFF. The state of the green output will return to the phase state every tenth second. To keep the output ON or OFF, the logic processor must turn it ON or OFF every tenth second.

SET PHASE RED 1-16 ON/OFF is the same as SET COB ON/OFF 32-47 respectively only sets the TS1 and TS2 Type 2 outputs. It is suggested that the Load Switch Red / Don't Walk channel also be set ON or OFF using **SET LDSW RED/DW 0-16 ON / OFF**

SET PHASE WALK 0-16 ON / OFF

Set the phase walk output ON or OFF. The state of the green output will return to the phase state every tenth second. To keep the output ON or OFF, the logic processor must turn it ON or OFF every tenth second.

SET PHASE WALK 1-16 ON/OFF is the same as SET COB ON/OFF 48-63 respectively and only sets the TS1 and TS2 Type 2 outputs. It is suggested that the Load Switch Green / Walk channel also be set ON or OFF using **SET LDSW GRN/WLK 0-16 ON / OFF**

SET PHASE PED CLR 0-16 ON / OFF

Set the phase pedestrian clearance output ON or OFF. The state of the green output will return to the phase state every tenth second. To keep the output ON or OFF, the logic processor must turn it ON or OFF every tenth second.

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Product Type: Controllers

ASC/3 Logic Processor Programming

SET PHASE PED CLR 1-16 ON/OFF is the same as SET COB ON/OFF 64-79 respectively and only sets theTS1 and TS2 Type 2 outputs. It is suggested that the Load Switch Yellow / Ped Clearance channel also be set ON or OFF using **SET LDSW YEL/PDCL 0-16 ON / OFF**

SET PHS DON'T WALK 0-16 ON / OFF

Set the phase don't walk output ON or OFF. The state of the green output will return to the phase state every tenth second. To keep the output ON or OFF, the logic processor must turn it ON or OFF every tenth second.

SET PHASE DON'T WALK 1-16 ON/OFF is the same as SET COB ON/OFF80-95 respectively only sets theTS1 and TS2 Type 2 outputs. It is suggested that the Load Switch Red / Don't Walk channel also be set ON or OFF using **SET LDSW RED/DW** 0-16 ON / OFF

OVERLAP OUTPUTS

(These outputs are for the selected overlap)

SET OVLP GREEN 0-16 ON / OFF

Set the overlap green output ON or OFF. The state of the green output will return to the phase state every tenth second. To keep the output ON or OFF, the logic processor must turn it ON or OFF every tenth second.

SET OVLP GREEN 1-16 ON/OFF is the same as SET COB ON/OFF 96-111 respectively and only sets the TS1 and TS2 Type 2 outputs. It is suggested that the Load Switch Green / Walk channel also be set ON or OFF using **SET LDSW GRN/WLK** 0-16 ON / OFF

SET OVLP YELLOW 0-16 ON / OFF

Set the overlap yellow output ON or OFF. The state of the green output will return to the phase state every tenth second. To keep the output ON or OFF, the logic processor must turn it ON or OFF every tenth second.

SET OVLP YELLOW 1-16 ON/OFF is the same as SET COB ON/OFF 112-127 respectively and only sets theTS1 and TS2 Type 2 outputs. It is suggested that the Load Switch Yellow / Ped Clearance channel also be set ON or OFF using **SET LDSW YEL/PDCL 0-16 ON / OFF. SET OVLEP RED** 0-16 ON / OFF

Set the overlap red output ON or OFF. The state of the green output will return to the phase state every tenth second. To keep the output ON or OFF, the logic processor must turn it ON or OFF every tenth second.

SET OVLP RED 1-16 ON/OFF is the same as SET COB ON/OFF 128-143 respectively only sets theTS1 and TS2 Type 2 outputs. It is suggested that the Load Switch Red / Don't Walk channel also be set ON or OFF using **SET LDSW RED/DW 0-16 ON / OFF**

LOAD SWITCH OUTPUTS

(These outputs are for the selected TS2 Type 1 Load Switch)

SET LDSW GRN/WLK 0-16 ON / OFF

Set the load switch green/walk output ON or OFF. The state of the green output will return to the phase state every tenth second. To keep the output ON or OFF, the logic processor must turn it ON or OFF every tenth second. Dimming is implemented according to MM-1-3 programming when the load switch is on.

SET LDSW GRN/WLK 1-16 ON/OFF is the same as SET COB ON/OFF 160-175 respectively. This sets the TS2 Type 1 Load Switch and does not set the TS1 or TS2 Type 2 outputs.







Product Type: Controllers

ASC/3 Logic Processor Programming

SET LDSW YEL/PCLR 0-16 ON / OFF

Set the load switch yellow/ped clear output ON or OFF. The state of the green output will return to the phase state every tenth second. To keep the output ON or OFF, the logic processor must turn it ON or OFF every tenth second. Dimming is implemented according to MM-1-3 programming when the load switch is on.

SET LDSW/PCLR 1-16 ON/OFF is the same as SET COB ON/OFF 176-191 respectively.

This sets the TS2 Type 1 Load Switch and does not set the TS1 or TS2 Type 2 outputs.

SET LDSW RED/DW 0-16 ON / OFF

Set the load switch red/don't walk output ON or OFF. The state of the green output will return to the phase state every tenth second. To keep the output ON or OFF, the logic processor must turn it ON or OFF every tenth second. Dimming is implemented according to MM-1-3 programming when the load switch is on.

SET LDSW RED/DW 1-16 ON/OFF is the same as SET COB ON/OFF 192-207 respectively. This sets the TS2 Type 1 Load Switch and does not set the TS1 or TS2 Type 2 outputs.

DETECTOR INPUTS (These inputs are for the selected detector)

SET VEH DET 1-16 1-16 ON / OFF Sets the "raw" vehicle detector 1-16 ON or OFF SET VEH DET 17-32 17-32 ON / OFF Sets the "raw" vehicle detector 17-32 ON or OFF SET VEH DET 33-48 33-48 ON / OFF Sets the "raw" vehicle detector 33-48 ON or OFF SET VEH DET 49-64 49-64 ON / OFF Sets the "raw" vehicle detector 49-64 ON or OFF SET PED DET 1-16 ON / OFF Sets the "raw" pedestrian detector 1-16 ON or OFF SET PED DET 1-16 ON is the same as SET CIB ON 64-79 respectively. SET PED DET 1-16 OFF is not the same as SET CIB OFF 64-79 respectively. If attempting to interrupt a pedestrian call and redirect it, use the SET CIB ON 64-79 ON/OFF executable statement.

PHASE INPUTS (These inputs are for the selected phase)

HOLD PHASE0-16ON / OFFTurn hold input ON or OFF to a selected phase (1-16) or all phases (0).OMIT PHASE0-16ON / OFFTurn omit input ON or OFF to a selected phase (1-16) or all phases (0).OMIT PED PHASE0-16ON / OFFTurn ped omit input ON or OFF to a selected phase (1-16) or all phases (0).

RING INPUTS (These inputs are for the selected ring)

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ASC/3 Logic Processor Programming ON / OFF SET INH MAX RING 0-4Turn inhibit max input ON or OFF to a selected ring (1-4) or all rings (0). SET MAX2 RING 0-4 ON / OFF Turn max 2 input ON or OFF to a selected ring (1-4) or all rings (0). SET MAX3 RING 0-4 ON / OFF Turn max 3 input ON or OFF to a selected ring (1-4) or all rings (0). OMIT RED CLR RING 0-4 ON / OFF Turn omit red clearance input ON or OFF to a selected ring (1-4) or all rings (0). SET RED REST RING 0-4 ON / OFF Turn red rest input ON or OFF to a selected ring (1-4) or all rings (0). SET PED REC RING ON / OFF 0-4 Turn pedestrian recycle input ON or OFF to a selected ring (1-4) or all rings (0). SET FORCE OFF RING ON / OFF 0-4 Turn force off input ON or OFF to a selected ring (1-4) or all rings (0). SET STOP TIME RING ON / OFF 0-4 Turn stop time input ON or OFF to a selected ring (1-4) or all rings (0). UNIT INPUTS (These are for the selected input) ON / OFF SET TEST A-E 0-5 Turn test inputs input ON or OFF for a selected test input (1-5) or all inputs (0). **SET CYCLE BIT 1-3** 0-3 ON / OFF Turn cycle bit inputs input ON or OFF for a selected cycle bit input (1-3) or all inputs (0). SET OFFSET BIT 1-3 ON / OFF 0-3 Turn offset bit inputs input ON or OFF for a selected offset bit input (1-3) or all inputs (0). SET SPLIT BIT 1-2 0-2 ON / OFF Turn split bit inputs input ON or OFF for a selected split bit input (1-2) or all inputs (0). SET ADDR BIT 0-4 0-4ON / OFF Turn address bit inputs input ON or OFF for a selected address bit input (1-3) or all inputs (0). SET IND LAMP CTRL ON / OFF Turn indicator lamp input ON or OFF SET EXTERNAL START ON / OFF Turn External Start input ON or OFF SET AUTO FLASH ON / OFF Turn auto flash input ON or OFF ON / OFF

SET LOCAL FLASH Turn local flash input ON or OFF

SET MMU FLASH ON / OFF

Turn MMU flash input ON or OFF **SET MMU STOP TIME** ON / OFF

Turn MMU stop time input ON or OFF

SET EXT TIME RESET ON / OFF Turn external time rest input ON or OFF

SET TBC ON LINE ON / OFF

Turn time base control input ON or OFF







Product Type: Controllers ASC/3 Logic Processor Programming SET DIMMING ENABLE ON / OFF Turn dimming enable input ON or OFF SET IM PWR SENSE ON / OFF Turn intersection monitor power sense input ON or OFF SET COORD SYNC ON / OFF Turn coordination sync input ON or OFF ON / OFF SET TLM EXT ADDR Turn telemetry external address enable input ON or OFF SET MAINT REQ'D ON / OFF Turn maintenance required (door open) input ON or OFF SET DIS PRETIME ON / OFF Turn disable pre-timed operation input ON or OFF SET TLM SPARE 1 ON / OFF Turn telemetry spare 1 input ON or OFF SET TLM SPARE 2 ON/OFF Turn telemetry spare 2 input ON or OFF 0-16 ON / OFF SET ALARM Turn input for selected alarms (1-16) or all alarms (0) ON or OFF. SET CNA 1 ON / OFF Turn CAN 1 (call to non-actuated) input ON or OFF ON / OFF **SET CNA 2** Turn CAN 2 (call to non-actuated) input ON or OFF00 SET WALK REST MOD ON / OFF Turn walk rest modifier input ON or OFF SET MIN RECALL ON / OFF Turn minimum recall input ON or OFF SET INT ADVANCE ON / OFF Turn interval advance input ON or OFF SET MAN CONTROL EN ON / OFF Turn manual control enable input ON or OFF SET STOP TIME ALL ON / OFF Turn stop time all rings input ON or OFF SET PH NEXT RX ON / OFF Turn phase next decision made in rex transfer input ON or OFF SET COORD FREE ON / OFF Turn coordination free input ON or OFF **SET SPLIT DEMAND 1** ON / OFF Turn split demand 1 input ON or OFF SET SPLIT DEMAND 2 ON / OFF Turn split demand 2 input ON or OFF SET DUAL COORD ON / OFF Turn dual coordination input ON or OFF CALL PREEMPT SEQ 0-10 ON/OFF

Turn input for selected (1-10) or all (0) preemptors ON or OFF.

SET PMT KBD LOCK 0-10 ON / OFF

Turn input from the keyboard for selected (1-10) or all (0) preemptors ON or OFF.





ASC/3 Logic Processor Programming

SET TSP CHKIN DET0-4ON / OFFTurns selected (1-4) or all (0) Transit Signal Priority check-in inputs ON or OFF.SET TSP CHKOUT DET0-4ON / OFFTurns selected (1-4) or all (0) Transit Signal Priority check-out inputs ON or OFF.SET PMT INTERLOCK0-10ON / OFFTurns selected (1-10) or all (0) preemption interlock inputs ON or OFF.

PHASE INPUTS (These inputs are for the selected phase)

CALL PHASE0-16ON / OFFTurns selected (1-16) or all (0) phase vehicle call inputs ON or OFF.CALL PED PHASE0-16ON / OFFTurns selected (1-16) or all (0) phase pedestrian call inputs ON or OFF.CALL BIKE PHASE0-16ON / OFFTurns selected (1-16) or all (0) phase bicycle call inputs ON or OFF.

UNIT INPUTS (These are for the selected input)

SET DB CRC

Turns selected (1-16) or all (0) data base CRC (Circular Redundant Check) inputs ON or OFF. **SET ALT SEQ A-E** 0-5 ON / OFF

Turns selected (1-5) or all (0) Alternate Sequence inputs ON or OFF.

0-16 ON/OFF

Use SET CIB CODE ON / OFF for locations 416 – 420 respectively for A-E. Sequence 1-32 is a BCD representation of A-E where E is highest. These inputs must be enabled in MM-1-1-1







esor Programming

Reference: AN2068 Date: March 14, 2007

ASC/3 Logic Processor Programming

Sequence	ALT SEQ E	ALT SEQ D	ALT SEQ C	ALT SEQ B	ALT SEQ A
1	OFF	OFF	OFF	OFF	ON
2	OFF	OFF	OFF	ON	OFF
3	OFF	OFF	OFF	ON	ON
4	OFF	OFF	ON	OFF	OFF
5	OFF	OFF	ON	OFF	ON
6	OFF	OFF	ON	ON	OFF
7	OFF	OFF	ON	ON	ON
8	OFF	ON	OFF	OFF	OFF
9	OFF	ON	OFF	OFF	ON
10	OFF	ON	OFF	ON	OFF
11	OFF	ON	OFF	ON	ON
12	OFF	ON	ON	OFF	OFF
13	OFF	ON	ON	OFF	ON
14	OFF	ON	ON	ON	OFF
15	OFF	ON	ON	ON	ON
16	ON	OFF	OFF	OFF	OFF
17	ON	OFF	OFF	OFF	ON
18	ON	OFF	OFF	ON	OFF
19	ON	OFF	OFF	ON	ON
20	ON	OFF	ON	OFF	OFF

SET TMGPLN BIT A-C 0-3 ON / OFF

Turns selected bits (1-3) or none (0) timing Plan Bit inputs ON or OFF.

```
Timing Plan 1 = 100, Plan 2 = 010, Plan 3 = 110 and Plan 4 = 001 Bits A-C respectively
Any other combination of Bits A.B.C result in the Timing plan called by the Time Base.
```

ENABLE DUAL ENTRY 0-63 ON / OFF

Turns enable dual entry input ON or OFF.

EN IDOT 5 SECT HD 0-63 ON / OFF

Turns enable IDOT 5 section head control input ON or OFF

SET PED2 DET 0-63 ON / OFF

Turns selected (1-16) or all (0) pedestrian 2 inputs ON or OFF.

```
TERM OVLP A-P NOW 0-16 ON / OFF
```

Turns selected (1-16) or all (0) terminate overlap now inputs ON or OFF.

To keep the overlap off, apply "OMIT OVLP A-P" at the same time.

OMIT OVLP A-P 0-16 ON / OFF

Turns selected (1-16) or all (0) overlap omit inputs ON or OFF.

CALL LOW PRI PMT 0-10 ON / OFF

Turns selected (1-10) or all (0) call low priority preemption inputs ON or OFF.

SET VEH PLAN A-C 0-3 ON / OFF

Turns selected (1-3) or all (0) vehicle detection plan inputs ON or OFF.

SET VEH DIAG A-C 0-3 ON / OFF

Turns selected (1-3) vehicle diagnostic plan inputs ON or OFF.

SET PED DIAG A-C 0-3 ON / OFF







ASC/3 Logic Processor Programming

Reference: AN2068 Date: March 14, 2007

Turns selected (1-3) pedestrian diagnostic plan inputs ON or OFF.

PHASE INPUTS (These inputs are for the selected phase)

SET PED EXT DET0-16ON / OFFTurns selected (1-16) or all (0) pedestrian extend detector inputs ON or OFF.SET RED EXT DET0-16ON / OFFTurns selected (1-16) or all (0) red extend inputs ON or OFF.CALL PED 20-16ON / OFFTurns selected (1-16) or all (0) phase pedestrian 2 inputs ON or OFF.

MISC STATES (Miscellaneous states)

SET CIB CODE OFF 0-575 Sets the selected CIB bit number (0-575) OFF. SET CIB CODE ON 0-575 Sets the selected CIB bit number (0-575) ON. SET COB CODE OFF 0-767 Sets the selected COB bit number (0-767) OFF. SET COB CODE ON 0-767 Sets the selected COB bit number (0-767) ON. (blank) This is a "Do Nothing" Statement.







Reference: AN2068 Date: March 14, 2007

ASC/3 Logic Processor Programming ASC3 CONTROLLER INPUT BUFFER (CIB)

CIB CODE	Signal Description	CIB CODE	Signal Description
0	Detector 1	16	Detector 17 (SD A1)
1	Detector 2	17	Detector 18 (SD A2)
2	Detector 3	18	Detector 19 (SD B1)
3	Detector 4	19	Detector 20 (SD B2)
4	Detector 5	20	Detector 21 (SD C1)
5	Detector 6	21	Detector 22 (SD C2)
6	Detector 7	22	Detector 23 (SD D1)
7	Detector 8	23	Detector 24 (SD D2)
8	Detector 9 (XD 1)	24	Detector 25
9	Detector 10 (XD 2)	25	Detector 26
10	Detector 11 (XD 3)	26	Detector 27
11	Detector 12 (XD 4)	27	Detector 28
12	Detector 13 (XD 5)	28	Detector 29
13	Detector 14 (XD 6)	29	Detector 30
14	Detector 15 (XD 7)	30	Detector 31
15	Detector 16 (XD 8)	31	Detector 32
32	Detector 33	48	Detector 49
33	Detector 34	49	Detector 50
34	Detector 35	50	Detector 51
35	Detector 36	51	Detector 52
36	Detector 37	52	Detector 53
37	Detector 38	53	Detector 54
38	Detector 39	54	Detector 55
39	Detector 40	55	Detector 56
40	Detector 41	56	Detector 57
41	Detector 42	57	Detector 58
42	Detector 43	58	Detector 59
43	Detector 44	59	Detector 60
44	Detector 45	60	Detector 61
45	Detector 46	61	Detector 62
46	Detector 47	62	Detector 63
47	Detector 48	63	Detector 64







ASC/3 Logic Processor Programming

CIB CODE	Signal Description	CIB CODE	Signal Description
64	Ped Detector 1	80	Phase 1 Hold
65	Ped Detector 2	81	Phase 2 Hold
66	Ped Detector 3	82	Phase 3 Hold
67	Ped Detector 4	83	Phase 4 Hold
68	Ped Detector 5	84	Phase 5 Hold
69	Ped Detector 6	85	Phase 6 Hold
70	Ped Detector 7	86	Phase 7 Hold
71	Ped Detector 8	87	Phase 8 Hold
72	Ped Detector 9	88	Phase 9 Hold
73	Ped Detector 10	89	Phase 10 Hold
74	Ped Detector 11	90	Phase 11 Hold
75	Ped Detector 12	91	Phase 12 Hold
76	Ped Detector 13	92	Phase 13 Hold
77	Ped Detector 14	93	Phase 14 Hold
78	Ped Detector 15	94	Phase 15 Hold
79	Ped Detector 16	95	Phase 16 Hold
96	Phase 1 Omit	112	Ped Omit Phase 1
97	Phase 2 Omit	113	Ped Omit Phase 2
98	Phase 3 Omit	114	Ped Omit Phase 3
99	Phase 4 Omit	115	Ped Omit Phase 4
100	Phase 5 Omit	116	Ped Omit Phase 5
101	Phase 6 Omit	117	Ped Omit Phase 6
102	Phase 7 Omit	118	Ped Omit Phase 7
103	Phase 8 Omit	119	Ped Omit Phase 8
104	Phase 9 Omit	120	Ped Omit Phase 9
105	Phase 10 Omit	121	Ped Omit Phase 10
106	Phase 11 Omit	122	Ped Omit Phase 11
107	Phase 12 Omit	123	Ped Omit Phase 12
108	Phase 13 Omit	124	Ped Omit Phase 13
109	Phase 14 Omit	125	Ped Omit Phase 14
110	Phase 15 Omit	126	Ped Omit Phase 15
111	Phase 16 Omit	127	Ped Omit Phase 16







ASC/3 Logic Processor Programming

CIB CODE	Signal Description		CIB CODE	Signal Description	
128	Inhibit Max Term	(R1)	144	Inhibit Max Term	(R3)
129	Max 2 Selection	(R1)	145	Max 2 Selection	(R3)
130	Max 3 Selection	(R1)	146	Max 3 Selection	(R3)
131	Omit Red Clear	(R1)	147	Omit Red Clear	(R3)
132	Red Rest	(R1)	148	Red Rest	(R3)
133	Ped Recycle	(R1)	149	Ped Recycle	(R3)
134	Force Off	(R1)	150	Force Off	(R3)
135	Stop Time	(R1)	151	Stop Time	(R3)
136	Inhibit Max Term	(R2)	152	Inhibit Max Term	(R4)
137	Max 2 Selection	(R2)	153	Max 2 Selection	(R4)
138	Max 3 Selection	(R2)	154	Max 3 Selection	(R4)
139	Omit Red Clear	(R2)	155	Omit Red Clear	(R4)
140	Red Rest	(R2)	156	Red Rest	(R4)
141	Ped Recycle	(R2)	157	Ped Recycle	(R4)
142	Force Off	(R2)	158	Force Off	(R4)
143	Stop Time	(R2)	159	Stop Time	(R4)
1.50			1.0.0		
160	Test A		176	Address Bit 0	
161 162	Test B Test C		177 178	Address Bit 1 Address Bit 2	
			178		
163	Test D		- • •	Address Bit 3	
164	Test E		180	Address Bit 4	
165	I/O Mode Bit A		181	Track Switch Fail	
166	I/O Mode Bit B		182	Ind. Lamp Control	
167	I/O Mode Bit C	7	183	External Start	laab
168	Cycle Bit 1 / TP Bit		184	Automatic (Remote) F	
169	Cycle Bit 2 / TP Bit	В	185	Flash Status/Local Fl	Lasn
170	Cycle Bit 3		186	MMU Status/CMU Flash	
171	Offset Bit 1		187	MMU (CMU) Stop Time	
172	Offset Bit 2		188	External Time Reset	
173	Offset Bit 3	a	189	TBC On Line	
174	Split Bit 1 / TP Bit		190	Dimming Enable	
175	Split Bit 2 / TP Bit	D	191	IM Power Sense	





Product Type: Controllers

ASC/3 Logic Processor Programming

CIB CODE	Signal Description		CIB CODE	Signal Description	
192	Coordinator Sync		208	Alarm 1	
193	TLM Extern Address Ena	able	209	Alarm 2	
194	TLM Maintenance Requir	red	210	Alarm 3	
195	Disable Pretimed Opera	ation	211	Alarm 4	
196			212	Alarm 5	
197			213	Alarm 6	
198	TLM Spare Input 1		214	Alarm 7	
199	TLM Spare Input 2		215	Alarm 8	
200			216	Alarm 9	
201			217	Alarm 10	
202			218	Alarm 11	
203			219	Alarm 12	
204			220	Alarm 13	
205			221	Alarm 14	
206			222	Alarm 15	
207			223	Alarm 16	
224	Call Non-Act I	(C1)	240	Call Non-Act I	(C2)
225	Call Non-Act II	(C1)	241	Call Non-Act II	(C2)
226	Walk-Rest Modifier	(C1)	242	Walk-Rest Modifier	(C2)
227	Minimum Recall	(C1)	243	Minimum Recall	(C2)
228	Interval Advance	(C1)	244	Interval Advance	(C2)
229	Manual Control Enable		245	Manual Control Enable	(C2)
230	Stop Time All Rings	(C1)	246	Stop Time All Rings	(C2)
231	Phase Next in RX	(C1)	247	Phase Next in RX	(C2)
232	Coordinator Free	(C1)	248	Coordinator Free	(C2)
233	Split Demand 1	(C1)	249	Split Demand 1	(C2)
234	Split Demand 2	(C1)	250	Split Demand 2	(C2)
235	Dual Coordination	(C1)	251	Dual Coordination	(C2)
236			252		
237			253		
238			254		
239			255		







ASC/3 Logic Processor Programming

CIB CODE	Signal Description		CIB CODE	Signal Description
256	Call Non-Act I	(C3)	272	Call Non-Act I (C4)
257	Call Non-Act II	(C3)	273	Call Non-Act II (C4)
258	Walk-Rest Modifier	(C3)	274	Walk-Rest Modifier (C4)
259	Minimum Recall	(C3)	275	Minimum Recall (C4)
260	Interval Advance	(C3)	276	Interval Advance (C4)
261	Manual Control Enable	(C3)	277	Manual Control Enable (C4)
262	Stop Time All Rings	(C3)	278	Stop Time All Rings (C4)
263	Phase Next in RX	(C3)	279	Phase Next in RX (C4)
264	Coordinator Free	(C3)	280	Coordinator Free (C4)
265	Split Demand 1	(C3)	281	Split Demand 1 (C4)
266	Split Demand 2	(C3)	282	Split Demand 2 (C4)
267	Dual Coordination	(C3)	283	Dual Coordination (C4)
268			284	
269			285	
270			286	
271			287	
288	Preempt 1 Call		304	KBD Locked Preempt 1 Call
289	Preempt 2 Call		305	KBD Locked Preempt 2 Call
290	Preempt 3 Call		306	KBD Locked Preempt 3 Call
291	Preempt 4 Call		307	KBD Locked Preempt 4 Call
292	Preempt 5 Call		308	KBD Locked Preempt 5 Call
293	Preempt 6 Call		309	KBD Locked Preempt 6 Call
294	Preempt 7 Call		310	KBD Locked Preempt 7 Call
295	Preempt 8 Call		311	KBD Locked Preempt 8 Call
296	Preempt 9 Call		312	KBD Locked Preempt 9 Call
297	Preempt 10 Call		313	KBD Locked Preempt 10 Call
298			314	
299			315	
300			316	TSP Check In Detector 1
301			317	TSP Check In Detector 2
302			318	TSP Check In Detector 3
303			319	TSP Check In Detector 4







ASC/3 Logic Processor Programming

320			Signal Description
320			
010	Preempt 1 Gate Down	336	Preempt 1 Interlock
321	Preempt 2 Gate Down	337	Preempt 2 Interlock
322	Preempt 3 Gate Down	338	Preempt 3 Interlock
323	Preempt 4 Gate Down	339	Preempt 4 Interlock
324	Preempt 5 Gate Down	340	Preempt 5 Interlock
325	Preempt 6 Gate Down	341	Preempt 6 Interlock
326	Preempt 7 Gate Down	342	Preempt 7 Interlock
327	Preempt 8 Gate Down	343	Preempt 8 Interlock
328	Preempt 9 Gate Down	344	Preempt 9 Interlock
329	Preempt 10 Gate Down	345	Preempt 10 Interlock
330	Reserved (OFF)	346	
331	Not Assigned (OFF)	2347	
332	TSP Check Out Detector 1	348	
333	TSP Check Out Detector 2	349	
334	TSP Check Out Detector 3	350	
335	TSP Check Out Detector 4	351	
352	Phase 1 Vehicle Call	368	Phase 1 Pedestrian Call
353	Phase 2 Vehicle Call	369	Phase 2 Pedestrian Call
354	Phase 3 Vehicle Call	370	Phase 3 Pedestrian Call
355	Phase 4 Vehicle Call	371	Phase 4 Pedestrian Call
356	Phase 5 Vehicle Call	372	Phase 5 Pedestrian Call
357	Phase 6 Vehicle Call	373	Phase 6 Pedestrian Call
358	Phase 7 Vehicle Call	374	Phase 7 Pedestrian Call
359	Phase 8 Vehicle Call	375	Phase 8 Pedestrian Call
360	Phase 9 Vehicle Call	376	Phase 9 Pedestrian Call
361	Phase 10 Vehicle Call	377	Phase 10 Pedestrian Call
362	Phase 11 Vehicle Call	378	Phase 11 Pedestrian Call
363	Phase 12 Vehicle Call	379	Phase 12 Pedestrian Call
364	Phase 13 Vehicle Call	380	Phase 13 Pedestrian Call
365	Phase 14 Vehicle Call	381	Phase 14 Pedestrian Call
366	Phase 15 Vehicle Call	382	Phase 15 Pedestrian Call
367	Phase 16 Vehicle Call	383	Phase 16 Pedestrian Call







ASC/3 Logic Processor Programming

CIB CODE	Signal Description	CIB CODE	Signal Description
384	Phase 1 Bike Call	400	Database CRC Bit 0
385	Phase 2 Bike Call	401	Database CRC Bit 1
386	Phase 3 Bike Call	402	Database CRC Bit 2
387	Phase 4 Bike Call	403	Database CRC Bit 3
388	Phase 5 Bike Call	404	Database CRC Bit 4
389	Phase 6 Bike Call	405	Database CRC Bit 5
390	Phase 7 Bike Call	406	Database CRC Bit 6
391	Phase 8 Bike Call	407	Database CRC Bit 7
392	Phase 9 Bike Call	408	Database CRC Bit 8
393	Phase 10 Bike Call	409	Database CRC Bit 9
394	Phase 11 Bike Call	410	Database CRC Bit 10
395	Phase 12 Bike Call	411	Database CRC Bit 11
396	Phase 13 Bike Call	412	Database CRC Bit 12
397	Phase 14 Bike Call	413	Database CRC Bit 13
398	Phase 15 Bike Call	414	Database CRC Bit 14
399	Phase 16 Bike Call	415	Database CRC Bit 15
416	Alt Sequence A	432	Ped 2 Detector 1
417	Alt Sequence B	433	Ped 2 Detector 2
418	Alt Sequence C	434	Ped 2 Detector 3
419	Alt Sequence D	435	Ped 2 Detector 4
420	Alt Sequence E	436	Ped 2 Detector 5
421	Timing Plan Bit A	437	Ped 2 Detector 6
422	Timing Plan Bit B	438	Ped 2 Detector 7
423	Timing Plan Bit C	439	Ped 2 Detector 8
424	Dual Entry Enable	440	Ped 2 Detector 9
425	Enable IDOT 5 Sec Head Ctl	441	Ped 2 Detector 10
426		442	Ped 2 Detector 11
427		443	Ped 2 Detector 12
428		444	Ped 2 Detector 13
429		445	Ped 2 Detector 14
430		446	Ped 2 Detector 15
431		447	Ped 2 Detector 16







ASC/3 Logic Processor Programming

CIB CODE Signal Description	on CIB C	ODE Signal Description
448 Overlap A Termi	nate Now 464	Overlap A Omit
449 Overlap B Termi	nate Now 465	Overlap B Omit
450 Overlap C Termi		Overlap C Omit
451 Overlap D Termi		Overlap D Omit
452 Overlap E Termi		Overlap E Omit
453 Overlap F Termi		Overlap F Omit
454 Overlap G Termi		Overlap G Omit
455 Overlap H Termi		Overlap H Omit
456 Overlap I Termi		Overlap I Omit
457 Overlap J Termi		Overlap J Omit
458 Overlap K Termi		Overlap K Omit
459 Overlap L Termi		Overlap L Omit
460 Overlap M Termi		Overlap M Omit
461 Overlap N Termi		Overlap N Omit
462 Overlap O Termi		Overlap O Omit
463 Overlap P Termi	nate Now 479	Overlap P Omit
480 Preempt 1 Low P	Priority Call 496	Veh Detector Plan Bit A
481 Preempt 2 Low P		Veh Detector Plan Bit B
482 Preempt 3 Low P		Veh Detector Plan Bit C
483 Preempt 4 Low P	Priority Call 499	
484 Preempt 5 Low P	Priority Call 500	
485 Preempt 6 Low P	Priority Call 501	
486 Preempt 7 Low P		Veh Detector Diag Plan Bit A
487 Preempt 8 Low P	Priority Call 503	Veh Detector Diag Plan Bit B
488 Preempt 9 Low P	-	Veh Detector Diag Plan Bit C
489 Preempt 10 Low P		Ped Detector Diag Plan Bit A
490	506	Ped Detector Diag Plan Bit B
491	507	Ped Detector Diag Plan Bit C
492	508	
493	509	
494	510	
495	511	







ASC/3 Logic Processor Programming

CIB CODE	Signal Description	CIB CODE Signal Description
512	Ped Extend Detector 1	528 Red Extend Detector 1
513	Ped Extend Detector 2	529 Red Extend Detector 2
514	Ped Extend Detector 3	530 Red Extend Detector 3
515	Ped Extend Detector 4	531 Red Extend Detector 4
516	Ped Extend Detector 5	532 Red Extend Detector 5
517	Ped Extend Detector 6	533 Red Extend Detector 6
518	Ped Extend Detector 7	534 Red Extend Detector 7
519	Ped Extend Detector 8	535 Red Extend Detector 8
520	Ped Extend Detector 9	536 Red Extend Detector 9
521	Ped Extend Detector 10	537 Red Extend Detector 10
522	Ped Extend Detector 11	538 Red Extend Detector 11
523	Ped Extend Detector 12	539 Red Extend Detector 12
524	Ped Extend Detector 13	540 Red Extend Detector 13
525	Ped Extend Detector 14	541 Red Extend Detector 14
526	Ped Extend Detector 15	542 Red Extend Detector 15
527	Ped Extend Detector 16	543 Red Extend Detector 16
	- 1 0 - 11 4	
544	Ped 2 Call 1	560
545	Ped 2 Call 2	561
546	Ped 2 Call 3	562
547	Ped 2 Call 4	563
548	Ped 2 Call 5	564
549	Ped 2 Call 6	565
550	Ped 2 Call 7	566
551	Ped 2 Call 8	567
552	Ped 2 Call 9	568
553	Ped 2 Call 10	569
554	Ped 2 Call 11	570
555	Ped 2 Call 12	571
556	Ped 2 Call 13	572
557	Ped 2 Call 14	573
558	Ped 2 Call 15	574
559	Ped 2 Call 16	575
L		







ASC/3 Logic Processor Programming

ASC3 CONTROLLER OUTPUT BUFFER (COB)

COB CODE	Signal Description	COB CODE	Signal Description
0	Phase 1 Green	16	Phase 1 Yellow
1	Phase 2 Green	17	Phase 2 Yellow
2	Phase 3 Green	18	Phase 3 Yellow
3	Phase 4 Green	19	Phase 4 Yellow
4	Phase 5 Green	20	Phase 5 Yellow
5	Phase 6 Green	21	Phase 6 Yellow
б	Phase 7 Green	22	Phase 7 Yellow
7	Phase 8 Green	23	Phase 8 Yellow
8	Phase 9 Green	24	Phase 9 Yellow
9	Phase 10 Green	25	Phase 10 Yellow
10	Phase 11 Green	26	Phase 11 Yellow
11	Phase 12 Green	27	Phase 12 Yellow
12	Phase 13 Green	28	Phase 13 Yellow
13	Phase 14 Green	29	Phase 14 Yellow
14	Phase 15 Green	30	Phase 15 Yellow
15	Phase 16 Green	31	Phase 16 Yellow
32	Phase 1 Red	48	Phase 1 Walk
33	Phase 2 Red	49	Phase 2 Walk
34	Phase 3 Red	50	Phase 3 Walk
35	Phase 4 Red	51	Phase 4 Walk
36	Phase 5 Red	52	Phase 5 Walk
37	Phase 6 Red	53	Phase 6 Walk
38	Phase 7 Red	54	Phase 7 Walk
39	Phase 8 Red	55	Phase 8 Walk
40	Phase 9 Red	56	Phase 9 Walk
41	Phase 10 Red	57	Phase 10 Walk
42	Phase 11 Red	58	Phase 11 Walk
43	Phase 12 Red	59	Phase 12 Walk
44	Phase 13 Red	60	Phase 13 Walk
45	Phase 14 Red	61	Phase 14 Walk
46	Phase 15 Red	62	Phase 15 Walk
47	Phase 16 Red	63	Phase 16 Walk







ASC/3 Logic Processor Programming

COB CODE	Signal Description	COB CODE	Signal Description
64	Phase 1 Ped Clear	80	Phase 1 Don't Walk
65	Phase 2 Ped Clear	81	Phase 2 Don't Walk
66	Phase 3 Ped Clear	82	Phase 3 Don't Walk
67	Phase 4 Ped Clear	83	Phase 4 Don't Walk
68	Phase 5 Ped Clear	84	Phase 5 Don't Walk
69	Phase 6 Ped Clear	85	Phase 6 Don't Walk
70	Phase 7 Ped Clear	86	Phase 7 Don't Walk
71	Phase 8 Ped Clear	87	Phase 8 Don't Walk
72	Phase 9 Ped Clear	88	Phase 9 Don't Walk
73	Phase 10 Ped Clear	89	Phase 10 Don't Walk
74	Phase 11 Ped Clear	90	Phase 11 Don't Walk
75	Phase 12 Ped Clear	91	Phase 12 Don't Walk
76	Phase 13 Ped Clear	92	Phase 13 Don't Walk
77	Phase 14 Ped Clear	93	Phase 14 Don't Walk
78	Phase 15 Ped Clear	94	Phase 15 Don't Walk
79	Phase 16 Ped Clear	95	Phase 16 Don't Walk
96	Overlap 1 Green	112	Overlap 1 Yellow
97	Overlap 2 Green	113	Overlap 2 Yellow
98	Overlap 3 Green	114	Overlap 3 Yellow
99	Overlap 4 Green	115	Overlap 4 Yellow
100	Overlap 5 Green	116	Overlap 5 Yellow
101	Overlap 6 Green	117	Overlap 6 Yellow
102	Overlap 7 Green	118	Overlap 7 Yellow
103	Overlap 8 Green	119	Overlap 8 Yellow
104	Overlap 9 Green	120	Overlap 9 Yellow
105	Overlap 10 Green	121	Overlap 10 Yellow
106	Overlap 11 Green	122	Overlap 11 Yellow
107	Overlap 12 Green	123	Overlap 12 Yellow
108	Overlap 13 Green	124	Overlap 13 Yellow
109	Overlap 14 Green	125	Overlap 14 Yellow
110	Overlap 15 Green	126	Overlap 15 Yellow
111	Overlap 16 Green	127	Overlap 16 Yellow







ASC/3 Logic Processor Programming

COB CODE	Signal Description	COB CODE	Signal Description
128	Overlap 1 Red	144	CF24 Det Slots 1,2 Reset
129	Overlap 2 Red	145	CF24 Det Slots 3,4 Reset
130	Overlap 3 Red	146	CF24 Det Slots 5,6 Reset
131	Overlap 4 Red	147	CF24 Det Slots 7,8 Reset
132	Overlap 5 Red	148	CF25 Det Slots 1,2 Reset
133	Overlap 6 Red	149	CF25 Det Slots 3,4 Reset
134	Overlap 7 Red	150	CF25 Det Slots 5,6 Reset
135	Overlap 8 Red	151	CF25 Det Slots 7,8 Reset
136	Overlap 9 Red	152	CF26 Det Slots 1,2 Reset
137	Overlap 10 Red	153	CF26 Det Slots 3,4 Reset
138	Overlap 11 Red	154	CF26 Det Slots 5,6 Reset
139	Overlap 12 Red	155	CF26 Det Slots 7,8 Reset
140	Overlap 13 Red	156	CF27 Det Slots 1,2 Reset
141	Overlap 14 Red	157	CF27 Det Slots 3,4 Reset
142	Overlap 15 Red	158	CF27 Det Slots 5,6 Reset
143	Overlap 16 Red	159	CF27 Det Slots 7,8 Reset
160	LS 1 Green/Walk	176	LS 1 Yellow/PC
161	LS 2 Green/Walk	177	LS 2 Yellow/PC
162	LS 3 Green/Walk	178	LS 3 Yellow/PC
163	LS 4 Green/Walk	179	LS 4 Yellow/PC
164	LS 5 Green/Walk	180	LS 5 Yellow/PC
165	LS 6 Green/Walk	181	LS 6 Yellow/PC
166	LS 7 Green/Walk	182	LS 7 Yellow/PC
167	LS 8 Green/Walk	183	LS 8 Yellow/PC
168	LS 9 Green/Walk	184	LS 9 Yellow/PC
169	LS 10 Green/Walk	185	LS 10 Yellow/PC
170	LS 11 Green/Walk	186	LS 11 Yellow/PC
171	LS 12 Green/Walk	187	LS 12 Yellow/PC
172	LS 13 Green/Walk	188	LS 13 Yellow/PC
173	LS 14 Green/Walk	189	LS 14 Yellow/PC
174	LS 15 Green/Walk	190	LS 15 Yellow/PC
175	LS 16 Green/Walk	191	LS 16 Yellow/PC







ASC/3 Logic Processor Programming

COB CODE	Signal Description	COB CODE	Signal Description
192	LS 1 Red/DW	208	LS 1 Green/Walk +
193	LS 2 Red/DW	209	LS 2 Green/Walk +
194	LS 3 Red/DW	210	LS 3 Green/Walk +
195	LS 4 Red/DW	211	LS 4 Green/Walk +
196	LS 5 Red/DW	212	LS 5 Green/Walk +
197	LS 6 Red/DW	213	LS 6 Green/Walk +
198	LS 7 Red/DW	214	LS 7 Green/Walk +
199	LS 8 Red/DW	215	LS 8 Green/Walk +
200	LS 9 Red/DW	216	LS 9 Green/Walk +
201	LS 10 Red/DW	217	LS 10 Green/Walk +
202	LS 11 Red/DW	218	LS 11 Green/Walk +
203	LS 12 Red/DW	219	LS 12 Green/Walk +
204	LS 13 Red/DW	220	LS 13 Green/Walk +
205	LS 14 Red/DW	221	LS 14 Green/Walk +
206	LS 15 Red/DW	222	LS 15 Green/Walk +
207	LS 16 Red/DW	223	LS 16 Green/Walk +
224	LS 1 Yellow/PC +	240	LS 1 Red/DW +
225	LS 2 Yellow/PC +	241	LS 2 Red/DW +
226	LS 3 Yellow/PC +	242	LS 3 Red/DW +
227	LS 4 Yellow/PC +	243	LS 4 Red/DW +
228	LS 5 Yellow/PC +	244	LS 5 Red/DW +
229	LS 6 Yellow/PC +	245	LS 6 Red/DW +
230	LS 7 Yellow/PC +	246	LS 7 Red/DW +
231	LS 8 Yellow/PC +	247	LS 8 Red/DW +
232	LS 9 Yellow/PC +	248	LS 9 Red/DW +
233	LS 10 Yellow/PC +	249	LS 10 Red/DW +
234	LS 11 Yellow/PC +	250	LS 11 Red/DW +
235	LS 12 Yellow/PC +	251	LS 12 Red/DW +
236	LS 13 Yellow/PC +	252	LS 13 Red/DW +
237	LS 14 Yellow/PC +	253	LS 14 Red/DW +
238	LS 15 Yellow/PC +	254	LS 15 Red/DW +
239	LS 16 Yellow/PC +	255	LS 16 Red/DW +







ASC/3 Logic Processor Programming

COB CODE	Signal Description	COB CODE	Signal Description
256	LS 1 Green/Walk -	272	LS 1 Yellow/PC -
257	LS 2 Green/Walk -	273	LS 2 Yellow/PC -
258	LS 3 Green/Walk -	274	LS 3 Yellow/PC -
259	LS 4 Green/Walk -	275	LS 4 Yellow/PC -
260	LS 5 Green/Walk -	276	LS 5 Yellow/PC -
261	LS 6 Green/Walk -	277	LS 6 Yellow/PC -
262	LS 7 Green/Walk -	278	LS 7 Yellow/PC -
263	LS 8 Green/Walk -	279	LS 8 Yellow/PC -
264	LS 9 Green/Walk -	280	LS 9 Yellow/PC -
265	LS 10 Green/Walk -	281	LS 10 Yellow/PC -
266	LS 11 Green/Walk -	282	LS 11 Yellow/PC -
267	LS 12 Green/Walk -	283	LS 12 Yellow/PC -
268	LS 13 Green/Walk -	284	LS 13 Yellow/PC -
269	LS 14 Green/Walk -	285	LS 14 Yellow/PC -
270	LS 15 Green/Walk -	286	LS 15 Yellow/PC -
271	LS 16 Green/Walk -	287	LS 16 Yellow/PC -
288	LS 1 Red/DW -	304	Phase 1 Detector Fail
289	LS 2 Red/DW -	305	Phase 2 Detector Fail
290	LS 3 Red/DW -	306	Phase 3 Detector Fail
291	LS 4 Red/DW -	307	Phase 4 Detector Fail
292	LS 5 Red/DW -	308	Phase 5 Detector Fail
293	LS 6 Red/DW -	309	Phase 6 Detector Fail
294	LS 7 Red/DW -	310	Phase 7 Detector Fail
295	LS 8 Red/DW -	311	Phase 8 Detector Fail
296	LS 9 Red/DW -	312	Phase 9 Detector Fail
297	LS 10 Red/DW -	313	Phase 10 Detector Fail
298	LS 11 Red/DW -	314	Phase 11 Detector Fail
299	LS 12 Red/DW -	315	Phase 12 Detector Fail
300	LS 13 Red/DW -	316	Phase 13 Detector Fail
301	LS 14 Red/DW -	317	Phase 14 Detector Fail
302	LS 15 Red/DW -	318	Phase 15 Detector Fail
303	LS 16 Red/DW -	319	Phase 16 Detector Fail







ASC/3 Logic Processor Programming

COB CODE	Signal Description	COB CODE	Signal Description
320	Phase 1 Timing	336	Phase 1 Next
321	Phase 2 Timing	337	Phase 2 Next
322	Phase 3 Timing	338	Phase 3 Next
323	Phase 4 Timing	339	Phase 4 Next
324	Phase 5 Timing	340	Phase 5 Next
325	Phase 6 Timing	341	Phase 6 Next
326	Phase 7 Timing	342	Phase 7 Next
327	Phase 8 Timing	2343	Phase 8 Next
328	Phase 9 Timing	344	Phase 9 Next
329	Phase 10 Timing	345	Phase 10 Next
330	Phase 11 Timing	346	Phase 11 Next
331	Phase 12 Timing	347	Phase 12 Next
332	Phase 13 Timing	348	Phase 13 Next
333	Phase 14 Timing	349	Phase 14 Next
334	Phase 15 Timing	350	Phase 15 Next
335	Phase 16 Timing	351	Phase 16 Next
352	Phase 1 Vehicle Check	368	Phase 1 Pedestrian Check
353	Phase 2 Vehicle Check	369	Phase 2 Pedestrian Check
354	Phase 3 Vehicle Check	370	Phase 3 Pedestrian Check
355	Phase 4 Vehicle Check	371	Phase 4 Pedestrian Check
356	Phase 5 Vehicle Check	372	Phase 5 Pedestrian Check
357	Phase 6 Vehicle Check	373	Phase 6 Pedestrian Check
358	Phase 7 Vehicle Check	374	Phase 7 Pedestrian Check
359	Phase 8 Vehicle Check	375	Phase 8 Pedestrian Check
360	Phase 9 Vehicle Check	376	Phase 9 Pedestrian Check
361	Phase 10 Vehicle Check	377	Phase 10 Pedestrian Check
362	Phase 11 Vehicle Check	378	Phase 11 Pedestrian Check
363	Phase 12 Vehicle Check	379	Phase 12 Pedestrian Check
364	Phase 13 Vehicle Check	380	Phase 13 Pedestrian Check
365	Phase 14 Vehicle Check	381	Phase 14 Pedestrian Check
366	Phase 15 Vehicle Check	382	Phase 15 Pedestrian Check
367	Phase 16 Vehicle Check	383	Phase 16 Pedestrian Check







ASC/3 Logic Processor Programming

COB CODE	Signal Description		COB CODE	Signal Description	
384	NEMA Status Bit A	(R1)	400	NEMA Status Bit A (R3)	
385	NEMA Status Bit B	(R1)	401	NEMA Status Bit B (R3)	
386	NEMA Status Bit C	(R1)	402	NEMA Status Bit C (R3)	
387	Coord Direction	(R1)	403	Coord Direction (R3)	
388			404		
389			405		
390			406		
391			407		
392	NEMA Status Bit A	(R2)	408	NEMA Status Bit A (R4)	
393	NEMA Status Bit B	(R2)	409	NEMA Status Bit B (R4)	
394	NEMA Status Bit C	(R2)	410	NEMA Status Bit C (R4)	
395	Coord Direction	(R2)	411	Coord Direction (R4)	
396			412		
397			413		
398			414		
399			415		
47.5			420		
416	Preemptor 1 Status		432	Cycle Bit 1 / TP Bit A	
417	Preemptor 2 Status		433	Cycle Bit 2 / TP Bit B	
418 419	Preemptor 3 Status		434	Cycle Bit 3 Offset Bit 1	
419	Preemptor 4 Status Preemptor 5 Status		435 436	Offset Bit 1 Offset Bit 2	
420	<u> </u>		436		
421	Preemptor 6 Status Preemptor 7 Status		437 438	Offset Bit 3 Split Bit 1 / TP Bit C	
422	Preemptor 7 Status Preemptor 8 Status		438 439	Split Bit 1 / TP Bit C Split Bit 2 / TP Bit D	
423	E E		439	SPIIC BIC 2 / IP BIC D	
424	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		440		
425 426	Preemptor 10 Status		441 442		
426 427			442		
427			443	Controller Select Bit A	
428	Droomptor Elach		444 445	Controller Select Bit A Controller Select Bit B	
429	Preemptor Flash FALSE (always logical	0.)	445	Controller Select Bit B Controller Select Bit C	
430	TRUE (always logical		446 447	Controller Select Bit C Controller Select Bit D	
101	INUE (AIWAYS IUGICAI	± /	11/	Concrotter Serect Bit D	







ASC/3 Logic Processor Programming

COB CODE	Signal Description		COB C	ODE Signal	l Description	
448 449 450 451 452 453 454 455 456 457 458 459 460 461 462 463	Crd Alarm Crd Error Crd Sync Out Crd X Street Sync Out Crd Free Status Crd No Fault Flash	(C1) (C1) (C1) (C1) (C1) (C1)	$\begin{array}{c} 464\\ 465\\ 466\\ 467\\ 468\\ 469\\ 470\\ 471\\ 472\\ 473\\ 474\\ 475\\ 476\\ 477\\ 478\\ 479\\ \end{array}$	Crd Crd Crd Crd	Alarm Error Sync Out X Street Sync Out Free Status No Fault Flash	(C2) (C2) (C2) (C2) (C2) (C2)
480 481 482 483 484 485 486 487 488 489 490 491 492 493 494 495	Crd Alarm Crd Error Crd Sync Out Crd X Street Sync Out Crd Free Status Crd No Fault Flash	(C3) (C3) (C3) (C3) (C3) (C3)	496 497 498 499 500 501 502 503 504 505 506 507 508 509 510 511	Crd Crd Crd Crd	Alarm Error Sync Out X Street Sync Out Free Status No Fault Flash	(C4) (C4) (C4) (C4) (C4) (C4)







ASC/3 Logic Processor Programming

COB CODE	Signal Description	COB CODE	Signal Description
512	NIC Special Function 1	528	Auxiliary 1
513	NIC Special Function 2	529	Auxiliary 2
514	NIC Special Function 3	530	Auxiliary 3
515	NIC Special Function 4	531	
516	NIC Special Function 5	532	
517	NIC Special Function 6	533	
518	NIC Special Function 7	534	
519	NIC Special Function 8	535	
520	TLM Special Function 1	536	Address Bit 0
521	TLM Special Function 2	537	Address Bit 1
522	TLM Special Function 3	538	Address Bit 2
523	TLM Special Function 4	539	Address Bit 3
524	TLM Special Function 5	540	Address Bit 4
525	TLM Special Function 6	541	
526	TLM Special Function 7	542	Voltage Monitor
527	TLM Special Function 8	543	Fault Monitor
544	Automatic (Remote) Flash	560	Coord Special Function 1
545	Preempt CMU Interlock	561	Coord Special Function 2
546	Flashing Logic 1 Hz	562	Coord Special Function 3
547	Flashing Logic 1.67 Hz	563	Coord Special Function 4
548	Flashing Logic 5 Hz	564	Coord Special Function 5
549		565	Coord Special Function 6
550	Local Flash Status	566	Coord Special Function 7
551	MMU Flash Status	567	Coord Special Function 8
552	No Fault Flash Status	568	Preempt Special Function 1
553		569	Preempt Special Function 2
554		570	Preempt Special Function 3
555		571	Preempt Special Function 4
556		572	Preempt Special Function 5
557		573	Preempt Special Function 6
558		574	Preempt Special Function 7
559		575	Preempt Special Function 8







ASC/3 Logic Processor Programming

COB CODE Signal Description	COB CODE Signal Description
576	592
577	593
578	594
579	595
580	596
581	597
582	598
583	599
584	600
585	601
587	602
588	603
589	604
590	605
591	606
	607
608	624
609	625
610	626
611	627
612	628
613	629
614	630
615	631
616	632
617	633
618	634
619	635
620	636
621	637
622	638
623	639







ASC/3 Logic Processor Programming

COB CODE Signal Description	COB CODE Signal Description
640	656
641	657
642	658
643	659
644	660
645	661
646	662
647	663
648	664
649	665
650	666
651	667
652	668
653	669
654	670
655	671
672	688
673	689
674	690
675	691
676	692
677	693
678	694
679	695
680	696
681	697
682	698
683	699
684	700
685	701
686	702
687	703
007	







ASC/3 Logic Processor Programming

COB CODE Signal Description	COB CODE Signal Description
704	720
705	721
706	722
707	723
708	724
709	725
710	726
711	727
712	728
713	729
714	730
715	731
716	732
717	733
718	734
719	735
736	752
737	753
738	754
739	755
740	756
741	757
742	758
743	759
744	760
745	761
746	762
747	763
748	764
749	765
750	766
751	767







Reference: AN2068 Date: March 14, 2007

ASC/3 Logic Processor Programming ASC/3 Extended Logic Processor Group

ASC/3 offers the users the ability to turn on and off a group of Logic Processor statements. These statements are in the range of 101-200 can be programmed by the Data Manager or on controller screen. You have to program allowable LP # range (group of LP) in the ASC3.ext file. Give it a name (LP feature 1) Then you can turn LP feature group 1 on and off using MM 2-6-2 Please note that the last LP group will precede the earlier group if the LP # is overlapped

Format

1. Comment statement

Line starts with " character will not be processed. This is used for putting comments in the file.

2. Message

Line starts with 'CONFIG='. Text after the '=' will be displayed in the sign-on screen and MM-2-6-2. Max number of characters is 12. This is optional.

eg: CONFIG=TOLEDO

3. Control statements

To specify which LP statements are allowed to be turned on or off. Max number of control statements is 25. The format is :

<on/off>,<start LP>,<end LP>,<Text>

<on/off> - 0=Turn off feature at power on

- 1=Turn on feature at power on
- <start LP> Starting LP statement. Range is from 101 200
- <end LP> Ending LP statement. Range is from 101 200
- <Text> Text is displayed in the MM-2-6-2 for the corresponding feature. Max length is 36 characters.

eg:

1,101,101,CANADIAN LEFT TURN

Layout of the MM-2-6-2

EXTENDED OPTIONS

EXTENDED FEATURES [TOLEDO] CANADIAN LEFT TURN...... ON FEATURE 2.....OFF

An ASC3.EXT can look like the below. Controller would translate and display them on MM-2-6-2

For further information, contact Econolite Technical Support	
800-225-6480x457 / 714-630-3700x457 / support@econolite.c	om







Reference: AN2068 Date: March 14, 2007

ASC/3 Logic Processor Programming

CONFIG=Santa Ana 1,101,106,LP FEATURE 1 0,107,111,LP FEATURE 2 0,112,113,CANADIAN LEFT TURN

1st group statement "LP FEATURE 1" specifies a group of LP statements from 101 and 106 that can be turned on or off together. Default is ON

1st group statement "LP FEATURE 2" specifies a group of LP statements from 107 and 111 that can be turned on or off together. Default is OFF

1st group statement "CANADIAN LEFT TURN" specifies a group of LP statements from 112 and 113 that can be turned on or off together. Default is OFF

MM-2-6-2 with ASC3.ext above in the controller at power up will display the following.

PRESS TOGGLE T	O CHANGE
PRESS TOGGLE T	1 2 3
MM SM ND NS	1 2 3 4 5 6
MM SM ND NS	1 2 3 4 5 6 7 8 9

